

Vitis あれこれ

ビルドフローを再確認

まずはリソースの準備

- vadd.cpp , host.cpp , host.hpp を用意
- design.cfg を用意

```
platform=xilinx_u50_gen3x16_xdma_201920_3
debug=1
profile_kernel=data:all:all:all
```

```
[connectivity]
nk=vadd:1:vadd_1
sp=vadd_1.in1:HBM[0]
sp=vadd_1.in2:HBM[1]
sp=vadd_1.out:HBM[2]
```

- xrt.ini を用意

```
[Debug]
profile=true
timeline_trace=true
data_transfer_trace=coarse # <coarse|fine|off>
```

でビルド

```
source /tools/Xilinx/Vitis/2019.2/settings64.sh
source /opt/xilinx/xrt/setup.sh
export platform=/opt/xilinx/platforms/xilinx_u50_gen3_x16_xdma_201920_3 /xilinx_u50_gen3_x16_xdma_201920_3.xpfm
g++ -I$XILINX_XRT/include ¥
    -I$XILINX_VIVADO/include ¥
    -Wall -O0 -g -std=c++11 ¥
    host.cpp -o host ¥
    -L$XILINX_XRT/lib -lOpenCL -lpthread -lrt -lstdc++
v++ -c -t hw --config design.cfg -k vadd -o vadd.xo vadd.cpp
vitis_analyzer vadd.xo.compile_summary
v++ -l -t hw --config design.cfg -o vadd.xclbin vadd.xo
vitis_analyzer vadd.xclbin.link_summary
./host vadd.xclbin
vitis_analyzer vadd.xclbin.run_summary
```

実行後のサマリを見ると HBM が 3 つぶらさがってる様子が確認できる .

参考

- <https://www.acri.c.titech.ac.jp/wordpress/archives/8355>
- https://xilinx.github.io/Vitis-Tutorials/2020-1/docs/my-first-program/cpp_kernel.html
- https://www.xilinx.com/html_docs/xilinx2020_2/vitis_doc/gnq1597858079367.html
- https://www.xilinx.com/html_docs/xilinx2020_1/vitis-guidance/HBM_USAGE.html
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