■ HEART(2)

Keynote: Beringing FPGAs to Production HPC Systems and Codes - Christian Plessl

FPGA: Heterogeneous Resource-Elastic Scheduling for CPU+FPGA Architectures - Anuj Vaishnav, Khoa Pham and Dirk Koch

- dynamically allocate CPUs and Reconfigurable resources to multiple tasks based on runtime conditions
- FPGA Shell: ZUCL "ZUCL: A zynq ultrascale+ framework for opencl hls applications" - <<< ReadItLater
- Spector benhmark で評価 https://ieeexplore.ieee.org/document/7929519 https://github.com/KastnerRG/spector
    - SDSoC-like な static scheduling とくらべて 2x speed up

FPGA: Physical Design Considerations for Synthesizable Standard-Cell-Based FPGAs

Scalable Filtering Modules for Database Acceleration on FPGAs - Kristiyan Manev, Anuj Vaishnav, Charalampos Kritikakis and Dirk Koch

- Database queris on FPGAs
    - convert query to static hardare <-> sysnthesis time is slow (unable to use at runtime for any query)
    - convert query to static hardare <-> limited programmability
    - -> partial runtime reconfiguration
- FPGA-Based Dynamically Reconfigurable SQL Query Processing と 比較. https://dl.acm.org/citation.cfm?id=2845087 <<< ReadItLater

Deep Learning Accelerator for an Intelligent Camera

- Optimization Techniques with Case studies
    - light-weight approach
    - probabilistic approach
    - systematic approach

- What's next
    - time sequence estimation
        - recurrent neural network
    - dataset generator
    - multi-task learning
        - taskonomy [Zamir, CVPR2018] https://arxiv.org/abs/1804.08328 <<< ReadItLater