

## 仕事

某社の日 .

## 一言メモ

- Thread Weaving: Static Resource Scheduling for Multithreaded High-Level Synthesis - <https://dl.acm.org/citation.cfm?id=3317924>
- Enabling Practical Processing in and near Memory for Data-Intensive Computing - <https://dl.acm.org/citation.cfm?id=3323476>
- Overcoming Data Transfer Bottlenecks in FPGA-based DNN Accelerators via Layer Conscious Memory Management - <https://dl.acm.org/citation.cfm?id=3317875>
- FPGA/DNN Co-Design: An Efficient Design Methodology for IoT Intelligence on the Edge - <https://dl.acm.org/citation.cfm?id=3317829>
- Dr. BFS: Data Centric Breadth-First Search on FPGAs - <https://dl.acm.org/citation.cfm?id=3317802>
- Open-Source EDA Tools and IP, A View from the Trenches - <https://dl.acm.org/citation.cfm?id=3323481>
- RISC-V Workshop Zurich Proceedings - <https://riscv.org/2019/06/risc-v-workshop-zurich-proceedings/>
- What You Synthesis is What You Simulate: Design of a RISC-V Core from C++ Specification - [https://content.riscv.org/wp-content/uploads/2019/06/16.45-Comet\\_Zurich\\_16-9.pdf](https://content.riscv.org/wp-content/uploads/2019/06/16.45-Comet_Zurich_16-9.pdf)
  - <https://gitlab.inria.fr/srokicki/Comet>
- Embench - <https://content.riscv.org/wp-content/uploads/2019/06/9.25-Embench-RISC-V-Workshop-Patterson-v3.pdf>
- Open Source Compiler Tool Chains and Operating Systems for RISC-V - <https://content.riscv.org/wp-content/uploads/2019/06/9.50-riscv-zurich-foss-compilers-os-12-jun-2019.pdf>
  - <https://github.com/cornell-brg/lizard>
  - <https://github.com/m-labs/nmigen/>
  - <https://github.com/lambdaconcept/minerva>
  - [https://github.com/westerndigitalcorporation/swerv\\_eh1](https://github.com/westerndigitalcorporation/swerv_eh1)
- Building Secure Systems Using RISC-V and Rust - [https://content.riscv.org/wp-content/uploads/2019/06/14.05-building\\_secure\\_systems-1.pdf](https://content.riscv.org/wp-content/uploads/2019/06/14.05-building_secure_systems-1.pdf)
- Compiling KB-sized machine learning models to tiny IoT devices - <https://dl.acm.org/citation.cfm?id=3314597>
  - <https://github.com/Microsoft/EdgeML/tree/master/Tools/SeeDot>
- High-level synthesis of functional patterns with Lift - <https://dl.acm.org/citation.cfm?id=3329957>
- HLS Backend Example - [https://github.com/dmlc/tvm/blob/master/docs/deploy/aws\\_fpga.md](https://github.com/dmlc/tvm/blob/master/docs/deploy/aws_fpga.md)
- ルーフラインモデルについてちょっと
  - ルーフラインモデルに基づくベクトルプロセッサ向けプログラム最適化戦略 - [https://ipsj.ixsq.nii.ac.jp/ej/index.php?action=pages\\_view\\_main&active\\_action=repository\\_action\\_common\\_download](https://ipsj.ixsq.nii.ac.jp/ej/index.php?action=pages_view_main&active_action=repository_action_common_download)
  - 計算機アーキテクチャを考慮した高効率画像処理プログラミング - [https://fukushima.web.nitech.ac.jp/paper/2017\\_ie\\_fukushima.pdf](https://fukushima.web.nitech.ac.jp/paper/2017_ie_fukushima.pdf)
  - The Roofline Model: A pedagogical tool for program analysis and optimization - [https://crd.lbl.gov/assets/pubs\\_presos/parlab08-roofline-talk.pdf](https://crd.lbl.gov/assets/pubs_presos/parlab08-roofline-talk.pdf)